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A Review of DC Fault Blocking Converters for HVDC Transmission Systems

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SUMMARY

Modular multilevel converters (MMCs) have emerged as the most promising candidate for use in voltage-sourced converter (VSC)-based high voltage direct current (HVDC) transmission systems due to substantial advantages when compared to two- and three-level VSCs. MMCs are comprised of stacks of submodules (SMs); the modular design allows MMCs to be easily adapted to higher voltage levels. Furthermore, output voltage and current of MMCs have negligible harmonics, thus reducing the need for AC-side filters. The simplest SM used in MMCs is the half-bridge SM (HBSM), consisting of a capacitor and two switches. However, similar to other VSCs, the HBSM-based MMC is unable to prevent the AC grid's contribution to DC-side fault currents. The use of circuit breakers (CBs) is required to protect HBSM-based MMCs. Direct current CBs (DCCBs) are expensive, while longer response times of the alternating current CBs (ACCBs) are not ideal for HVDC systems' protection. An innovative solution to this problem is the use of SMs that are capable of blocking the AC side contribution to the DC-side fault current in MMCs.

The addition of two extra switches to the HBSM structure results in the full-bridge SM (FBSM) configuration. The presence of these switches ensures that in the event of a DC fault, the reverse voltage from the FBSM capacitor is in the path of the AC side current feeding the DC side fault through the antiparallel diodes. However, the presence of additional semiconductor switches in each SM results in doubling the conduction losses as well as an increase in the device cost. To mitigate these problems, several SM configurations have been proposed in recent years that provide DC fault blocking capability with lower losses and device count than those associated with FBSMs. This has given rise to a class of DC fault blocking converters. In this paper, noteworthy DC fault blocking SM configurations are reviewed and compared in terms of component requirements, the number of switches in the conduction path, fault blocking symmetry and over-modulation capability. Certain fault blocking SMs that provide additional benefits in terms of reducing the number of voltage sensors and switch voltage ratings are investigated as well.

KEYWORDS

Modular multilevel converter (MMC), DC fault blocking, submodule (SM), high voltage direct current (HVDC) transmission

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1. INTRODUCTION

The use of voltage-sourced converter (VSC) in high voltage direct current (HVDC) transmission offers greater flexibility when compared to its counterpart, the line commutated converter (LCC), due to its smaller footprint, as well as decoupled active and reactive power control, voltage support provision and black-start capability. The most recent advances in VSC technology has resulted in the emergence of a new converter topology known as the modular multilevel converter (MMC). MMCs address many of the limitations encountered in convectional VSCs, such as scalability to higher voltages by the addition of more levels, provision of smooth output voltage waveforms at a lower switching frequency, and elimination of low-order harmonics which typically require large filters [1]. MMCs are comprised of stacks of cells or submodules (SMs). The simplest and most economical cell structure is the half-bridge SM (HBSM) which consists of a capacitor and two switches. Similar to other VSC-HVDC systems, the HBSM-based MMC is unable to prevent AC side contribution to DC-side faults. DC circuit breakers (DCCBs) may be used to clear such faults, but DCCB technology is neither mature nor cost-effective. The use of alternating current CBs (ACCBs) on the AC side is another option. However, ACCBs take a few cycles to trip and are not adequately fast for HVDC system protection. A more effective way to protect HVDC systems is to use SMs with fault blocking capability in the MMC structure.

The full-bridge SM (FBSM) developed by the addition of two switches to the HBSM structure is capable of such fault blocking operation. However, it has nearly double the conduction losses and device count when compared to the HBSM. Several SM configurations have been proposed over the years that provide DC fault blocking capability with lower losses and device count than FBSM, giving rise to a class of DC fault blocking converters. Section 2 of this paper describes the operation of HBSM- and FBSM-based MMCs during normal operation and faults; it also explains how over-modulation in MMC requires the use of bipolar SMs. Section 3 reviews several fault blocking SMs and compares them based on features such as the number of switches in the conduction path, device count, over-modulation capability and fault blocking symmetry. Comparisons with regards to voltage ratings of IGBT switches and voltage sensor requirements are also made where appropriate. Section 4 discusses the findings and Section 5 draws some conclusions.

2. SYSTEM STRUCTURE AND OPERATION

Figure 1(a) shows a general representation of a three-phase MMC. Each leg of the converter is comprised of two arms and each arm consists of N series-connected SMs along with an arm inductor. The arm inductors serve a dual purpose of limiting fault currents as well as filtering high-frequency components in the circulating current. The SMs consist of switches and capacitor(s) capable of producing two or more voltage levels. The SMs can be modelled as voltage sources that can be either bypassed or inserted into the arm current path. Each arm of the MMC is capable of generating the full DC link voltage, V_{dc}. The number of inserted SMs in the upper and lower arms is varied to generate an alternating multilevel waveform at the AC terminal. The phase a terminal voltage, v_a, in Figure 1(a) may be expressed in either one of the following ways:

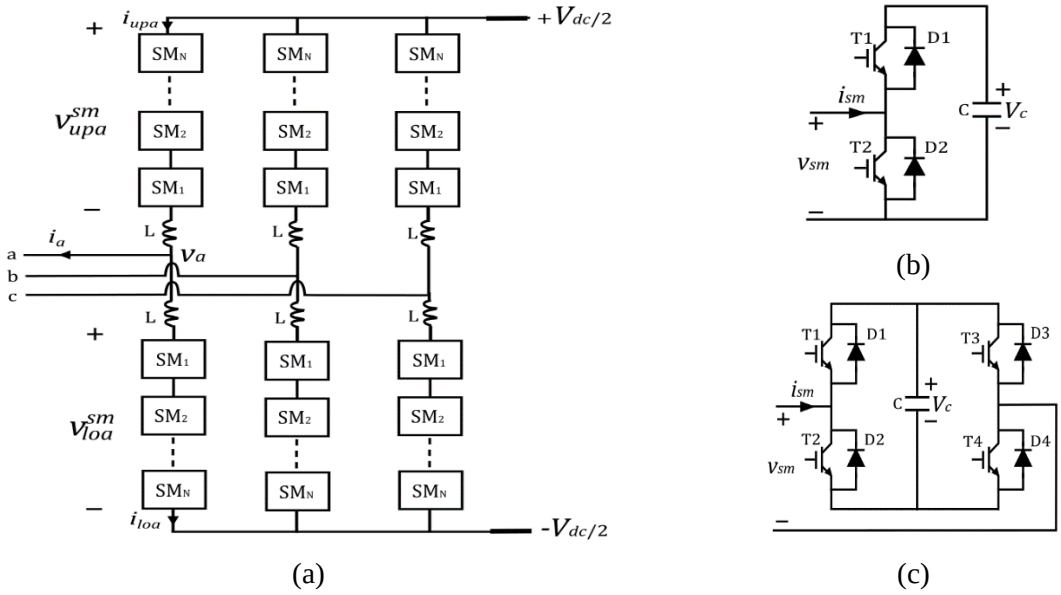
$$v_a = \frac{V_{dc}}{2} - v_{upa}^{sm} - L\frac{di_{upa}}{dt}, \tag{1}$$

$$v_a = -\frac{V_{dc}}{2} + v_{loa}^{sm} + L\frac{di_{loa}}{dt}, \tag{2}$$

where v_{upa}^{sm}, v_{loa}^{sm} are the total upper and lower arm SM voltages while i_{upa}, i_{loa} are the upper and lower arm currents of phase a. Since the upper and lower arm voltages vary between 0 and V_{dc}, the peak value of the AC voltage, $\hat{V}_a$ is equal to $V_{dc}/2$. The modulation index, *m*, is defined as the ratio of the peak AC voltage to half of the DC link pole-to-pole voltage:

$$m = \frac{\hat{V}_a}{0.5V_{dc}}. \tag{3}$$

According to (3), operating in the over-modulation region, i.e., operating with a modulation index greater than 1, is possible if SMs can generate negative voltages. Over-modulation is necessary to maintain the AC voltage when the DC link voltage is reduced [2].



(a) (b) (c)

Figure 1: (a) Structure of a three-phase MMC (b) Half-bridge submodule (HBSM) and (c) Full-bridge submodule (FBSM)

The HBSM shown in Figure 1(b) is capable of generating two voltage levels, 0 and V_c, by the complementary switching of the IGBT switches T1 and T2 as shown in Table 1. Lack of availability of a negative voltage state means that the modulation index is limited to a maximum value of 1 (or 1.15 with selective harmonic elimination). By contrast, the FBSM shown in Figure 1(c) can generate three voltage levels, 0, V_c and $-V_c$, as shown in Table 2. Hence, the FBSM is a bipolar SM that can generate negative voltage states not only during fault blocking but also during normal operation, which is a useful feature if the over-modulation capability is required in the converter.

Table 1: HBSM switching states

Operating Mode	T1	T2	i_{sm}	v_{sm}
Blocked	0	0	>0	V_c
Blocked	0	0	<0	0
Bypassed	0	1	-	0
Inserted	1	0	-	V_c

Table 2: FBSM switching states

Operating Mode	T1	T2	T3	T4	i_{sm}	v_{sm}
Blocked	0	0	0	0	>0	V_c
Blocked	0	0	0	0	<0	$-V_c$
Bypassed	0	1	0	1	-	0
Bypassed	1	0	1	0	-	0
Inserted	1	0	0	1	-	V_c
Inserted	0	1	1	0	-	$-V_c$

When a fault occurs on the DC side of an HBSM-based MMC, the initial current surge is due to the discharge of the SM capacitors through the IGBTs. After fault detection, all IGBT switches are blocked to prevent damages to the switches. This prevents the further discharge of the capacitors. However, depending on the type of SM used, the AC grid may still feed the DC-side fault.

Taking the case of a pole-to-ground fault in the HBSM-MMC as an example, when the SM current is positive (i_{sm}>0 in Figure 2(a)), diode D1 and the capacitor C in each of the SMs are in the fault current path (path through IGBTs is now blocked). The total capacitor voltage of N HBSMs in each MMC arm equals V_{dc}. Meanwhile, the peak ac voltage is equal to $V_{dc}/2$ from (1) and (2). Since the reverse voltage generated by the MMC arm is greater than the peak ac grid phase voltage, diode D1 is reverse biased and the fault current is suppressed. However, when the current direction reverses (Figure 2(b)), the SM capacitors are bypassed entirely and no reverse voltage is inserted by the SM capacitors in the current path. Therefore, the AC-side source feeds the pole-to-ground fault on the DC side.

Considering the case of a pole-to-pole fault in the HBSM-based MMC, the fault current from a particular phase enters one of the arms, circulates through the fault and returns via a different arm into another phase. For i_{sm}>0, the reverse voltage provided by each MMC arm still equals V_{dc} but since two arms are in operation, the total reverse voltage in the fault current path is $2V_{dc}$. At the same time, the peak AC-side voltage that needs to be considered in this case is the line-to-line voltage peak ($\sqrt{3}*V_{dc}/2$) since two phases are involved. Once again, as the reverse voltage from the MMC arms is greater than the peak-to-peak AC voltage, the fault current is suppressed. However, when the SM current direction reverses, all HBSM capacitors are bypassed and the AC line voltage feeds the pole-to-pole fault. From this discussion, it can be concluded that regardless of the type of the fault, the HBSM is only able to block the fault current contribution from the AC grid for exactly half a cycle; there is an uncontrolled AC current flowing into the DC-side fault during the other half cycle.

From the FBSM structure shown in Figure 1(c) it is clear that the presence of the two additional IGBTs along with their antiparallel diodes ensures that regardless of the arm current direction, the capacitor in each SM is inserted with opposite polarity in the fault current path when a DC-side fault occurs and all IGBTs in the SMs are blocked. This fault blocking process is illustrated in Figures 2(c)-(d).

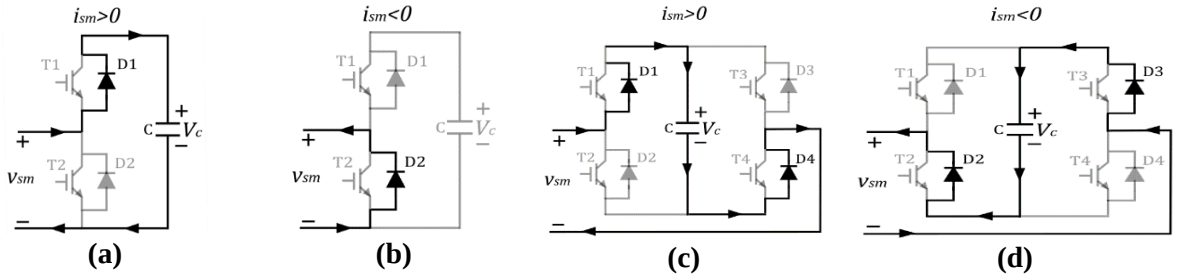


Figure 2: Fault current path through (a) HBSM for i_{sm}>0 (b) HBSM for i_{sm}<0 (c) FBSM for i_{sm}>0 (d) FBSM for i_{sm}<0

3. SUBMODULE CONFIGURATIONS

In the following subsections, based on a literature review, the pros and cons of several noteworthy proposed SM configurations, with fault blocking capability, for MMC, will be discussed.

3.1 Unipolar Full Bridge Submodule (UFBSM): The UFBSM proposed in [3] is derived by removing one IGBT from the standard FBSM (Figure 3(a)). The SM capacitor voltage is equal to V_{dc}/N (considering N SMs per arm).

Removal of the IGBT results in a slightly lower device count when compared to the FBSM, with the same conduction losses. In this configuration, the unidirectional nature of diode D3 implies that the SM cannot insert a negative voltage in the circuit during normal operation and hence over-modulation is not possible. The fault blocking operation remains identical to that of the FBSM. The output voltage of the SM, v_{sm}, during the DC fault blocking mode, is shown in Figure 3(a) for both directions of SM current. For i_{sm}>0, diodes D1 and D4 and capacitor C are in the current path. Similarly, diodes D2 and D3 and capacitor C are in the fault current path when i_{sm}<0.

3.2 Diode Clamp Submodule (DCSM): Figure 3(b) illustrates the configuration of the DCSM proposed in [4]. The addition of two diodes (D3 and D4) and an IGBT (T3) to a standard half-bridge SM forms the DCSM. The total number of switches in DCSM is identical to the UFBSM. Similar to the UFBSM, the DCSM does not support the bipolar operation. Even though there are two capacitors in the SM, only two voltage states are available during the normal operation, as the capacitors cannot be inserted individually into the current path. Either the SM is bypassed or both capacitors are inserted. So, to make a fair comparison with the other topologies, the total voltage across the two capacitors in the SM is taken to be V_c. With identical capacitors, the voltage across each capacitor would then be V_{dc}/2N.

During normal operation, T3 is on at all times. So, there are two switches in the conduction path just as is the case of the FBSM. Upon detection of a DC-side fault, all IGBTs in the SM are turned off. When the SM current is positive, the fault response is similar to that of a standard HBSM. Both capacitors are inserted into the circuit to oppose the flow of the current; a total reverse voltage of V_{dc} is therefore generated by each arm. For the negative SM current direction, with T3 turned off, the current is directed through diode D4, thus eliminating the freewheeling effect of diode D2. This change inserts capacitor C2 into the current path, which blocks the fault current. An asymmetry is observed during fault operation. For i_{sm}>0, both capacitors C1 and C2 are utilized during fault blocking and the reverse voltage per arm is V_{dc}. When i_{sm}<0, only capacitor C2 and consequently V_{dc}/2 per arm is available for fault blocking (assuming capacitors C1 and C2 have voltages $V_{C1}=V_{C2}=0.5V_c$ in each SM). This reverse voltage is the minimum required to block the fault current during DC-side pole-to-ground faults since the AC voltage peak is equal to V_{dc}/2 as explained previously. Such an asymmetry during fault blocking operation can lead to longer fault current suppression times [5].

The advantage of this SM is that the blocking voltage across the additional devices (T3, D3 and D4) only needs to be V_{dc}/2N, i.e., half the maximum SM voltage. The UFBSM and the FBSM on the other hand, require all switches to be capable of blocking the full SM voltage.

3.3 Clamped Double Submodule (CDSM): The CDSM [5] shown in Figure 3(c) is the equivalent of two HBSMs connected through a switch and two diodes. The CDSM contains two capacitors and can generate three voltage states, 0, V_c and $2V_c$. For a fair comparison between various SM configurations, the CDSM needs to be considered as the equivalent of two series-connected single capacitor SMs such as HBSM, UFBSM, FBSM or DCSM. (Note that DCSM is considered a single capacitor SM, as each of its capacitors has a voltage of $0.5V_c$ across it).

Similar to the UFBSM, the CDSM is incapable of generating negative voltages during normal operation. Two FBSMs use a total of four switches to generate any of the voltage states, while the CDSM requires only three switches to be in the conduction path to insert both SM capacitors into the current path; this implies that conduction losses are reduced with the CDSM.

During faults, both capacitors block the flow of the fault current when the SM current direction is positive. For the negative current direction, the capacitors C1 and C2 are connected in parallel and hence the reverse voltage generated per arm is V_{dc}/2. The equivalent circuit of a CDSM-MMC during a pole-to-pole DC-side fault is shown in Figure 4.

3.4 Switched Capacitor Submodule (SCSM): The SCSM [6] was proposed to reduce control complexity in addition to providing fault blocking for DC-side faults. It does not support bipolar operation and provides asymmetrical fault blocking as shown in Figure 3(d). The voltage states 0 and $2V_c$ are obtained through four switches. So, conduction losses would be similar to that of the FBSM. The V_c state may be obtained with the insertion of either one of the capacitors C1 or C2 into the circuit using three switches. It may be also realized by inserting both capacitors in parallel which would increase the number of conducting switches to five. The primary purpose of this module is in the reduction of the number of voltage sensors in the MMC, as explained below.

There are voltage balancing and sorting algorithms in place that ensure that SMs' capacitor voltages remain approximately constant and equal during MMC operation. For instance, the widely implemented algorithm in [7] sorts the capacitor voltages in the order of magnitude. Afterwards, depending upon the arm current direction and the required level of arm voltage, certain capacitors with the lowest (highest) voltage magnitudes are selected to be in the current path to be charged (discharged). This implies that the voltages of all capacitors need to be monitored which is accomplished using voltage sensors. Hence,

the total number of sensors equals the number of capacitors in the SMs. The measurement of all capacitor voltages requires a significantly high number of voltage sensors for voltage balancing, particularly for MMCs with a large number of SMs. For the SCSM, the parallel connection of the two capacitors ensures both capacitors are at the same voltage. Thus, only one voltage sensor per SM is enough to monitor the capacitor voltages. However, the realization of this parallel mode comes at the expense of having five switches in the conduction path.

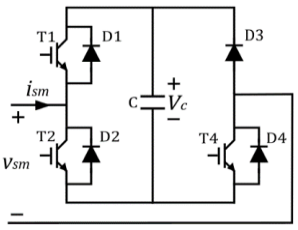
3.5 Semi Full Bridge Submodule (SFBSM): The SFBSM proposed in [8] and illustrated in Figure 3(e) was derived from the CDSM. Both diodes in the CDSM have been replaced by active switches to make bipolar SM. There are four voltage states, 0, V_c, -V_c and 2V_c. This configuration also allows the two capacitors in the SM to be connected in parallel with both positive and negative polarities which helps with voltage balancing, thus reducing the total number of required voltage sensors. This is an improvement over the SCSM in the sense that the generation of all voltage states requires the use of one fewer switch. Hence, on-state losses are comparable to the CDSM, as three switches are sufficient to realize output voltage levels of 0, - V_c, V_c and 2V_c. Only the parallel connection mode of the capacitors requires the use of four switches. The fault blocking operation remains asymmetrical, as in the SCSM, with only capacitor C1 available to block the fault when the SM current direction is negative.

3.6 Three-Level Cross Connected Submodule (TLCCSM): The TLCCSM proposed in [9] is essentially two HBSMs connected in series through a clamp circuit, as shown in Figure 3(f). The SM can utilize both capacitors to suppress the fault current leading to symmetrical DC fault blocking. During normal operation, switches T5 and T6 are always operational and the SM can generate three voltage levels, 0, V_c and 2V_c. Due to the presence of the diodes in the clamp circuit, negative voltage states are not possible. Four switches are operational for the synthesis of all possible voltage states, leading to conduction losses that are comparable to that of the FBSM. There is a slight reduction in device cost when compared to the FBSM, as two of the IGBT switches are replaced with diodes.

3.7 Five-Level Cross Connected Submodule (FLCCSM): The FLCCSM [10] shown in Figure 3(g) is made up of two HBSMs cross-connected through two switches. FLCCSM can generate five output voltage levels, 0, V_c, 2V_c, -V_c and -2V_c. Bipolar voltage outputs enable the SMs to operate in the over-modulation region when required. Only three switches are needed in the conduction path during normal operation. Hence, conduction losses are comparable to that of the CDSM. A major disadvantage of the FLCCSM is that the clamp switches need to tolerate the voltages of both SM capacitors and therefore may require a series connection of two switches, which would result in higher conduction losses.
[11] proposes the series-connected double SM (SDSM) which is derived from the FLCCSM by removing T6 and making the switch unidirectional. This results in a slight reduction in device count while keeping DC fault blocking operation symmetric; however, the SM becomes unipolar.

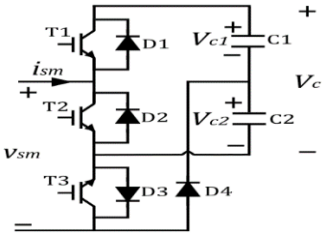
3.8 Asymmetrical Full Bridge Submodule (AFBSM): The AFBSM, proposed in [12], has a total of four switches in its SM, as shown in Figure 3(h). As the name implies, DC fault blocking is asymmetrical. The SM is bipolar and generates a total of four voltage states, 0, V_c, 2V_c and -V_c. Only capacitor C1 can be used for the negative SM voltage output. During normal operation, two switches need to be in the conduction path to attain the four voltage states; hence, the main advantage of this topology is its low conduction losses. However, switches T1 and T2 need to be able to tolerate the voltages of both capacitors in the circuit. So, they will either need to be rated for higher voltages or a series connection of two switches may be required, which would lead to increased conduction losses.

3.9 Mixed Submodule: The mixed submodule (Figure 3(i)) presented in [13] is a series connection of an HBSM and an FBSM. It provides asymmetrical DC fault blocking and has the over-modulation capability. Four voltage levels may be generated during normal operation (0, V_c, -V_c, 2V_c). These voltage states require the use of three switches and thus on-state conduction losses are expected to be the same as those in the CDSM. However, when compared to the CDSM, it has one extra IGBT and one fewer diode, resulting in a slight increase in the semiconductor device cost.



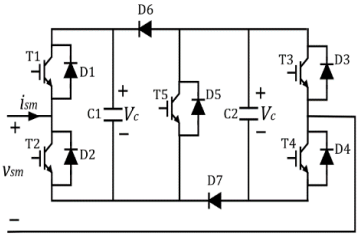
Blocking State	
i_{sm}	v_{sm}
>0	V_c
<0	$-V_c$

(a) Unipolar Full Bridge Submodule (UFBSM)



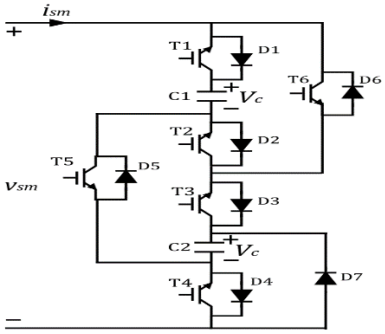
Blocking State	
i_{sm}	v_{sm}
>0	$V_{c1}+ V_{c2}= V_c$
<0	$-V_{c2}$

(b) Diode Clamp Submodule (DCSM)



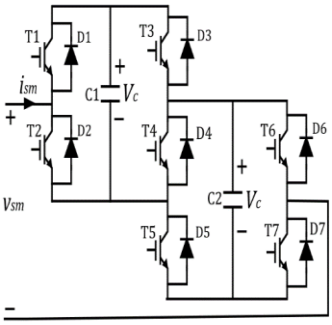
Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-V_c$

(c) Clamped Double Submodule (CDSM)



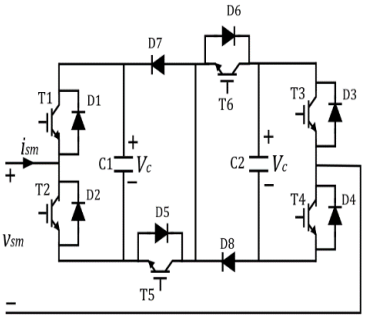
Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-V_c$

(d) Switched Capacitor Submodule (SCSM



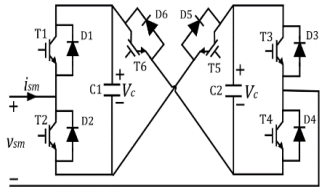
Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-V_c$

(e) Semi Full Bridge Submodule (SFBSM)



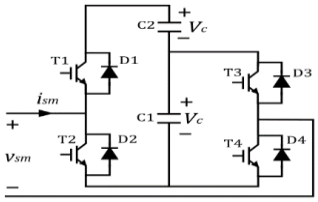
Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-2V_c$

(f) Three-Level Cross Connected Submodule (TLCCSM)



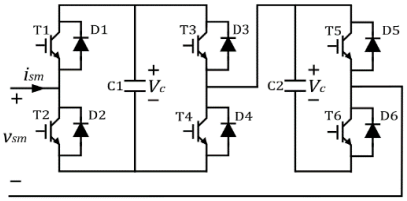
Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-2V_c$

(g) Five-Level Cross Connected Submodule (FLCCSM)



Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-V_c$

(h) Asymmetrical Full Bridge Submodule (AFBSM)



Blocking State	
i_{sm}	v_{sm}
>0	$2V_c$
<0	$-V_c$

(i) Mixed Submodule

Figure 3: Submodule configurations and blocking voltage levels

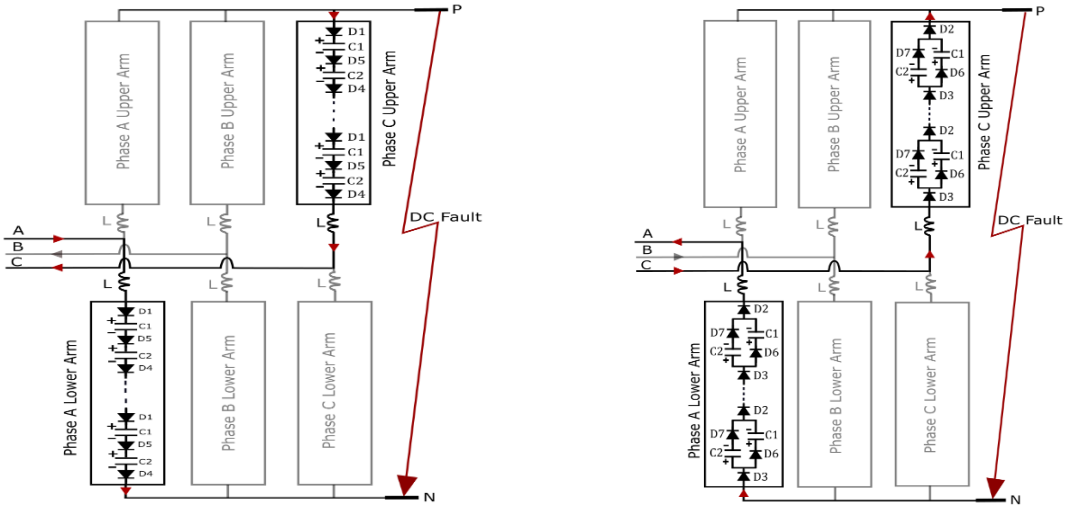


Figure 4: Fault current path for a pole-to-pole fault in the CDSM-MMC showing one phase for (a) $i_{sm} > 0$ and (b) $i_{sm} < 0$

4. DISCUSSION

In terms of assistance with voltage balancing and a reduced number of voltage sensors, topologies such as the SFBSM and SCSM that allow parallel connection of capacitors are desirable. For lower conduction losses, the AFBSM is preferred, but the voltage rating of the IGBT switches need to be higher, which increases the SM cost. Besides, fault blocking in the AFBSM is asymmetrical leading to inferior performance. The FLCCSM provides over-modulation capability along with symmetrical fault blocking. However, the same problem with the voltage rating of IGBT switches exists in this configuration. The CDSM and the mixed SM are comparable to the FLCCSM in terms of device count and conduction losses, but are only capable of realizing unipolar voltage outputs; therefore, over-modulation is not possible with these SMs. The characteristics of the fault blocking SMs are summarized in Table 3.

TABLE 3: Characteristics of different fault blocking SMs

	FBSM (2 SMs)	UFBSM (2 SMs)	DCSM (2 SMs)	CDSM	SCSM	SFBSM	TLCCSM	FLCCSM	AFBSM	Mixed SM
No of IGBTS	8	6	6	5	6	7	6	6	4	6
No of diodes	8	8	8	7	7	7	8	6	4	6
No of switches in the conduction path (V0/V1/V2*)	4/4/4	4/4/4	4/4/4	3/3/3	4/5/4	3/4/3	4/4/4	3/3/3	2/2/2	3/3/3
No of voltage sensors	2	2	2	2	1	1	2	2	2	2
Over-modulation	Yes	No	No	No	No	Yes	No	Yes	Yes	Yes
Symmetrical DC fault blocking	Yes	Yes	No	No	No	No	Yes	Yes	No	No

*** V0/V1/V2 denotes voltage states of 0, V_c and $2V_c$ in the SMs.**

5. CONCLUSION

In this paper, a variety of SM configurations with DC fault blocking capability were reviewed and compared against each other. Some topologies hold an advantage in terms of lower conduction losses or total semiconductor device count, while others may provide better performance if voltage balancing capability and control complexity are considered. If over-modulation is required, the mixed SM and the AFBSM are suitable choices. The SFBSM is a proper candidate if a lower number of voltage sensors along with reduced control complexity is desired. Hence, the decision on implementing a certain SM configuration for an MMC in a particular HVDC converter station would depend on the system requirements.

BIBLIOGRAPHY

[1] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell and B. W. Williams, "New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System," in IEEE Transactions on Power Systems, vol. 28, no. 1, pp. 335-346, Feb. 2013.

[2] N. Thitichaiworakorn, M. Hagiwara and H. Akagi, "Experimental verification of a modular multilevel cascade inverter based on double-star bridge-cells (MMCI-DSBC)," 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, 2012, pp. 4196-4202.

[3] J. Qin, M. Saeedifard, A. Rockhill and R. Zhou, "Hybrid Design of Modular Multilevel Converters for HVDC Systems Based on Various Submodule Circuits," in IEEE Transactions on Power Delivery, vol. 30, no. 1, pp. 385-394, Feb. 2015.

[4] X. Li, W. Liu, Q. Song, H. Rao and S. Xu, "An enhanced MMC topology with DC fault ride-through capability," IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society, Vienna, 2013, pp. 6182-6188.

[5] R. Marquardt, “Modular multilevel converter: An universal concept for HVDC-networks and extended DC-bus-applications,” in Proc. Int. Power Electron. Conf., Jun. 2010, pp. 502–507.

[6] A. A. Elserougi, A. M. Massoud and S. Ahmed, "A Switched-Capacitor Submodule for Modular Multilevel HVDC Converters With DC-Fault Blocking Capability and a Reduced Number of Sensors," in IEEE Transactions on Power Delivery, vol. 31, no. 1, pp. 313-322, Feb. 2016.

[7] M. Saeedifard and R. Iravani, "Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System," in IEEE Transactions on Power Delivery, vol. 25, no. 4, pp. 2903-2912, Oct. 2010.

[8] K. Ilves, L. Bessegato, L. Harnefors, S. Norrga and H. -. Nee, "Semi-full-bridge submodule for modular multilevel converters," 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, 2015, pp. 1067-1074.

[9] R. Li, J. E. Fletcher, L. Xu, D. Holliday and B. W. Williams, "A Hybrid Modular Multilevel Converter With Novel Three-Level Cells for DC Fault Blocking Capability," in IEEE Transactions on Power Delivery, vol. 30, no. 4, pp. 2017-2026, Aug. 2015.

[10] A. Nami, L. Wang, F. Dijkhuizen and A. Shukla, "Five level cross connected cell for cascaded converters," 2013 15th European Conference on Power Electronics and Applications (EPE), Lille, 2013, pp. 1-9.

[11] J. Zhang and C. Zhao, "The Research of SM Topology With DC Fault Tolerance in MMC-HVDC," in IEEE Transactions on Power Delivery, vol. 30, no. 3, pp. 1561-1568, June 2015.

[12] A. Nami, J. Liang, F. Dijkhuizen and G. D. Demetriades, "Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 18-36, Jan. 2015. [12]R. Marquardt, “Modular multilevel converter: An universal concept for HVDC-networks and extended DC-bus-applications,” in Proc. Int. Power Electron. Conf., Jun. 2010, pp. 502–507.

[13] G. Adam, K. Ahmed, and B. Williams, "Mixed cells modular multilevel converter," in Industrial Electronics (ISIE), 2014 IEEE 23rd International Symposium on, 2014, pp. 1390-1395.