IEC 61850-Based FLISR Testing: A Comparative Study using RTDS

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SUMMARY

This paper outlines the implementation, testing and performance comparison of two protection schemes used for Fault Location, Isolation, and Service Restoration (FLISR) in modern distribution feeders, namely:

- Scheme 1: A vendor-specific communication-enhanced protection coordination scheme for auto-reclosers (ARs) using Curve-Shifting Coordination (CSC) automation platform, versus
- Scheme 2: A non-proprietary and highspeed protection coordination scheme which uses IEC61850-based communications (using GOOSE messages).

The key objectives of the tests and performance analysis were to capture the maximum time required for fault detection and clearing using GOOSE message communications and to investigate the expected response of inverter-based DERs during a fault on a study feeder.

A typical utility feeder was used as the study model in a lab environment for the benchmarking and comparison analysis of the two schemes. The protection coordination tests were carried out by applying faults at pre-defined locations in order to verify the coordination between the relays associated with backbone ARs and to verify the ride-through capabilities of a battery energy storage system (BESS) inverter supplying the feeder customers. Testing of scheme 1 protection coordination was carried out in a real-time digital simulation environment implemented with the RSCAD software tool. To test and verify scheme 2, three SEL relays (SEL-651R, SEL-751A and SEL-351A) with GOOSE messaging functionality were interfaced with the real-time testing environment (RTDS®) using a control hardware-in-the-loop (CHIL) testing.

The results obtained from the testing of Scheme 1 showed that the average time taken for an AR to coordinate with an upstream AR through simulated CSC was approximately 40 ms, which comprises of both the communication and processing time. On the other hand, upstream relay coordination with GOOSE messaging could be achieved on average in approximately 9 ms. In addition to being able to block the upstream relay faster, using IEC61850-based communications can also provide value in enhancing trip time of the downstream relay, through a permissive or direct transfer trip (DTT) scheme, instead of relying on loss of potential tripping for isolating a faulty section. Consequently, if the upstream relay is blocked and the downstream relay has been tripped through a permissive signal, the upstream relay closest to the fault can immediately operate, instead of relying on conventional timed-overcurrent tripping for coordination which can be slow. Faster fault detection and clearing can also lead to conditions where DERs can now effectively ride-through fault scenarios for any downstream or adjacent feeder fault, to improve performance.

Therefore, even in the case where the upstream shift signal used in the vendor-specific scheme can be made faster through enhancing communication media that have faster speeds (lower latency), using IEC61850-based communications can offer more comprehensive and versatile protection coordination schemes, agnostic to relay vendors, power system topologies, and outside of proprietary methods.

KEYWORDS

Protection relay testing, IEC 61850, GOOSE, hardware-in-the-loop, communication assisted protection scheme, real-time digital simulation.

INTRODUCTION

Applications of IEC61850 GOOSE for distribution feeder protection are still new and in development; however, a few examples such as permissive schemes and DTT method have already emerged and proven to improve protection automation performance and to reduce overall fault clearing time [1]. The value provided by the high speed, peer-to-peer communication protocol to traditional protection schemes is outlined by the authors in [2]. A real-time hardware-in-the-loop simulation (HIL) is used when parts of a simulation model are replaced with physical devices, in order to evaluate the device's response to power system behaviour and events. Authors in [3] describe the procedure for HIL testing and the validation of overcurrent relays through HIL testing is discussed in [4].

The key objective of the tests outlined in this paper is to capture the time for fault detection, processing, communication and clearing using fault detection and clearing method based on GOOSE messaging and to verify the expected ride-through response of inverter-based DERs. A comparison is made with performance of a vendor-specific Curve-Shifting Coordination (CSC) scheme that is presently used for fault clearing and coordination of multiple auto-reclosers on a distribution feeder. The tests conducted in a HIL manner have been used to capture the timing throughout the process of fault inception, detection, clearing, and service restoration. In addition, voltage and current waveforms (event records) at selected points across the distribution feeder were also recorded for analysis and comparison.

PROTECTION PHILOSOPHY OVERVIEW

Scheme 1 - Curve-Shifting Protection Coordination

Figure 1 shows the communication-enhanced curve-shifting protection coordination scheme using a vendor-specific method given a fault at location #1. The expected operation using this protection philosophy is that AR B trips as the direct upstream AR to the fault and AR B sends a curve shift signal to AR A to shift to a slower TOC curve, effectively inhibiting operation. The downstream AR to the fault location, AR C, is expected to trip on loss of potential.

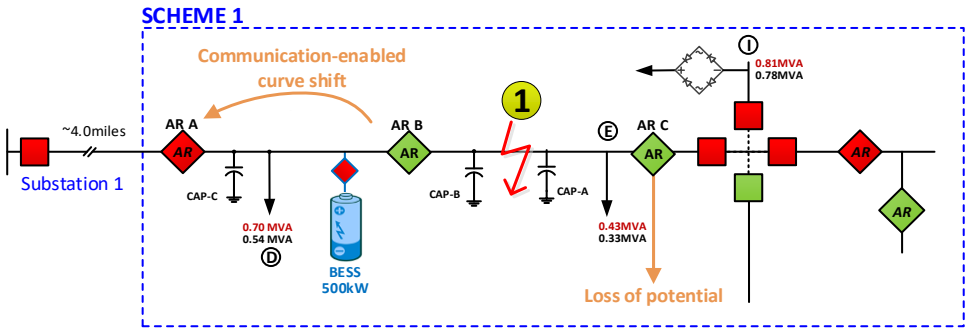

Figure 1. Simulated CSC-based protection coordination

Scheme 2 – IEC61850-Based Protection Coordination

Figure 2 shows the proposed protection coordination scheme enabled through IEC61850-based communication. The expected operation for a fault at location #1 is that AR B blocks the operation of AR A. Then, AR B and AR C operate after a permissive trip signal is sent to AR C.

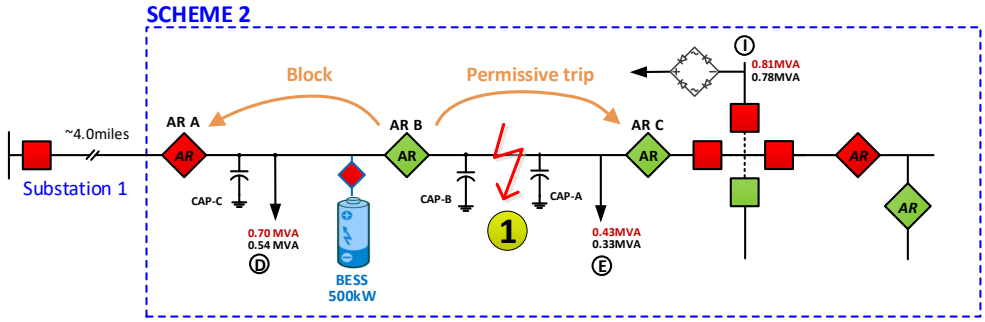

Figure 2. IEC61850-based protection coordination

BESS Ride-Through Protection Settings

The study system includes a battery energy storage system (BESS) as an example of an inverter-based DER on a distribution feeder. The BESS has been modelled with voltage and frequency ride-through capabilities, based on [5]. Table 1 outlines the voltage and frequency ride-through settings that were implemented for this study.

Table 1. BESS Voltage and Frequency Ride-Through Settings

Region	*Voltage Range (% of nominal voltage)*	*Operation Mode*	*Minimum Ride-Through Time (s)*	*Maximum Trip Time (s)*
High Voltage 2	$V \geq 120$	Cease to energize	N/A	0.16
High Voltage 1	$110 < V < 120$	Mandatory operation	12	13
Near Nominal Voltage	$88 \leq V \leq 110$	Continuous operation	Infinite	N/A
Low Voltage 1	$70 \leq V \leq 88$	Mandatory operation	20	21
Low Voltage 2	$50 \leq V \leq 70$	Mandatory operation	10	11
Low Voltage 3	$V < 50$	Mandatory operation	1	1.5

Region	*System Frequency Default Settings*	*Ride-Through Operation Mode*	*Ride-Through Until (s)*	*Maximum Trip Time (s)*
High Frequency 2	$f > 62$	N/A	No ride-through	0.16
High Frequency 1	$60.5 < f < 62$	Mandatory operation	299	300
Near Nominal	$58.5 \leq f \leq 60.5$	Continuous operation	Indefinite	N/A
Low Frequency 1	$57.0 \leq f < 58.5$	Mandatory operation	299	300
Low Frequency 2	$f < 57.0$	N/A	No ride-through	0.16

CURVE-SHIFTING PROTECTION COORDINATION STUDY

This section provides the detailed protection design and conventional relay settings that were simulated in RSCAD with respect to AR A, AR B and AR C for a fault at a location #1. The primary protection present on AR A and AR B is timed-overcurrent protection. For a fault at location #1, it is expected that AR B trips for the fault whereas AR A remains closed. The protection coordination between AR A and AR B is implemented as shown in Table 2 and Figure 3 where TOC1 is a faster curve than the shifted TOC2 curve.

Table 2. TOC Curve Settings

	TOC Type	*Pickup Current Primary (A)*	*CT Ratio (1000A / 5A)*	*Pickup Current Secondary (A)*	*Time Dial*	*Curve*
Phase	TOC1 (Normal)	600	200	3	1.2	U3 (IEEE US - Very Inverse)
Neutral	TOC1 (Normal)	400	200	2	2.5	U3 (IEEE US - Very Inverse)
Phase	TOC2 (Shifted)	600	200	3	4	U1 (IEEE US - Moderately Inverse)
Neutral	TOC2 (Shifted)	400	200	2	8	U1 (IEEE US - Moderately Inverse)

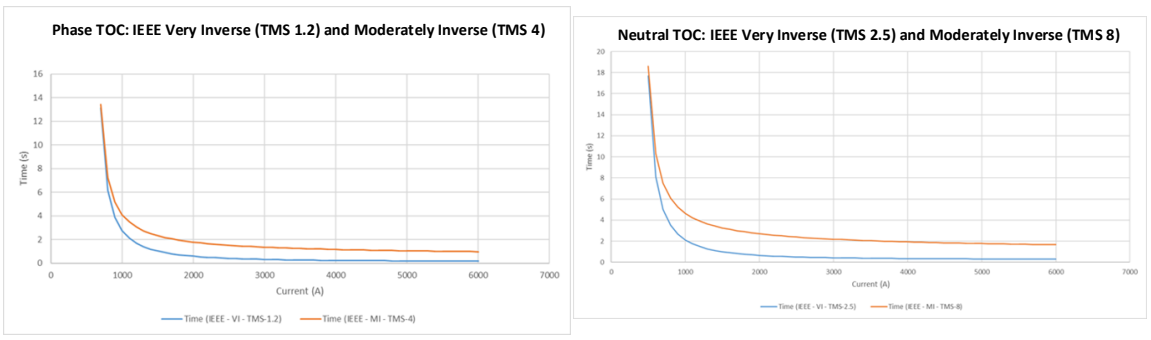

Figure 3. Normal and shifted TOC curves for phase and neutral settings

In order to effectively block the operation of the upstream relay, AR A, the TOC curves are shifted from the normal curve to a slower TOC2 curve using the IOC pickup of AR B as the shifting signal. The IOC settings of AR B are shown in Table 3.

Table 3. Instantaneous Phase Overcurrent Settings

Pickup current – primary (A)	1200
Pickup current – secondary (A)	6

Additionally, AR A, AR B and AR C also contain loss of potential settings as outlined in Table 4 where a relay would trip provided that the grid-side voltage is below 50% for 30 seconds.

Table 4. Loss of Potential Settings

Pickup voltage	50% (50% of PT secondary)
Delay	30 seconds
PT ratio	12.47 V / 120 V (L-L) (Ratio: 103.917)

For the purposes of this study, breaker operating time is assumed to be 2 cycles (based on AR vacuum fault interrupters). A communication delay of 2 cycles (32 ms) is assumed to account for the delay in hardwired connections in the CSC-based protection scheme.

Curve-Shifting Protection Coordination Results

For the purpose of testing the scheme 1 protection coordination scheme, two sets of three-phase-to-ground (LLLG) faults, line-to-line (LL) faults and line-to-ground (LG) faults were applied, with a zero fault impedance and a 2 ohm fault impedance. All faults were for a duration of 500 cycles. Table 5 shows that AR B and AR C tripped for a bolted LLLG fault at location 1 and AR A remains closed. Note that the BESS disconnects for the bolted LLLG fault, as shown in Figure 4.

Table 5. Trip Times and Communication Delays for Bolted LLLG Fault (Scheme 1)

AR A Trip Time (s)	*AR B Trip Time (s)*	*AR C Trip Time (s)*	*BESS Trip Time (s)*	*Pickup time for AR B IOC element (s)*	*Time for TOC shift to AR A (s)*
N/A	0.2917	30.06	0.2321	0.0051	0.0386

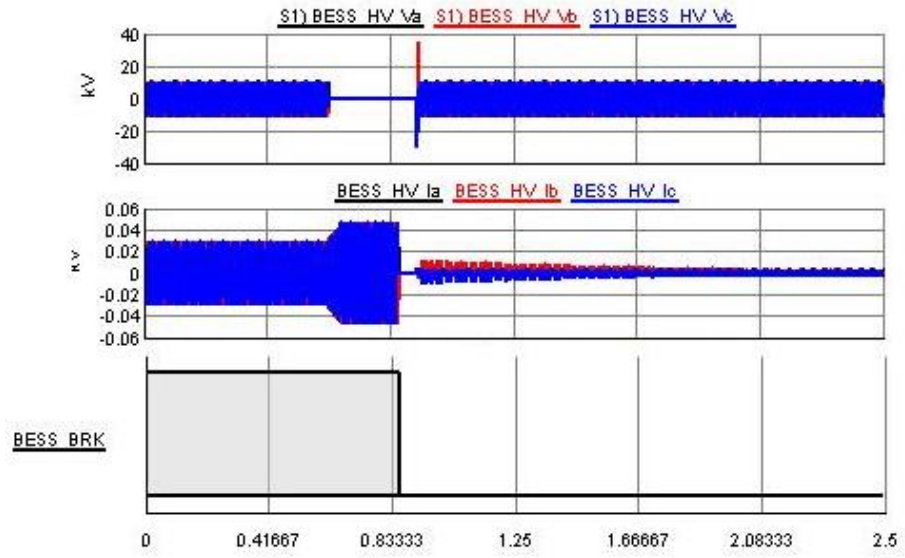

Figure 4. BESS - Bolted LLLG - Voltage, current and breaker status at HV terminal (Scheme 1)

IEC61850-BASED PROTECTION CO-ORDINATION STUDY

Hardware-in-the-Loop Testbed Setup

To study the protection coordination scheme using IEC61850-based communication, three SEL relays capable of IEC61850 communication were incorporated in a HIL test with the RTDS. SEL-351A is used as the relay for AR A, SEL-651R as the relay for AR B and SEL-751A as the relay for AR C. Figure 5 shows the lab testbed setup where the SEL relays interface with the RTDS and the user.

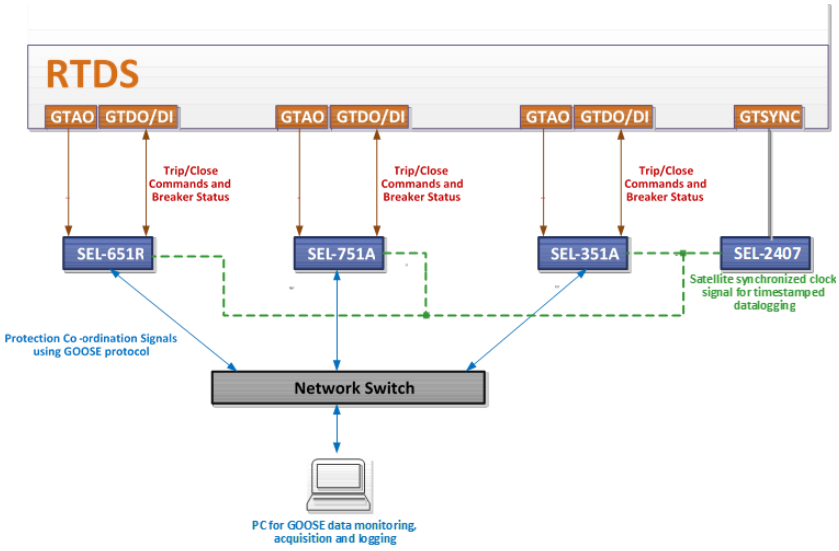

Figure 5. Hardware-in-the-loop testbed setup schematic

Protection Design and HIL Relay Settings with GOOSE Messaging

The following list and Table 6 summarize the GOOSE communication architecture used to establish the protection co-ordination scheme among the HIL relays.

SEL-351A (AR A) – GOOSE Architecture

- Subscribes to the IOC pickup element from SEL-651R (AR B)
- Publishes the acknowledgment signal for the AR A block

SEL-651R (AR B) – GOOSE Architecture

- Subscribes to the acknowledgment signal for the AR A block
- Subscribes to the IOC element pickup from SEL-751A (AR C)
- Publishes the IOC element pickup of AR B
- Publishes the logic signal which is true when the IOC of AR B has picked up, AR A has been blocked and the IOC element of AR C has not picked up

SEL-751A (AR C) – GOOSE Architecture

- Subscribes to logic signal from SEL-651R (AR B)
- Publishes the IOC element pickup of AR C

Table 6. GOOSE Communication Architecture

<table>
<tr><td colspan="3" rowspan="2"></td><td colspan="4">Subscribers</td></tr>
<tr><td>351A (AR A)</td><td colspan="2">651R (AR B)</td><td>751A (AR C)</td></tr>
<tr><td>AR B_IOC</td><td>AR A_BLOCK_ACK</td><td>AR C_IOC</td><td>AR B_IOC * AR A_BLOCK_ACK * !(AR C_IOC)</td></tr>
<tr><td rowspan="4">Publishers</td><td rowspan="2">351A (AR A)</td><td>AR A_BLOCK_ACK</td><td>N/A</td><td>X</td><td></td><td></td></tr>
<tr><td rowspan="2">651R (AR B)</td><td>AR B_IOC</td><td>X</td><td colspan="2" rowspan="2">N/A</td><td></td></tr>
<tr><td>AR B_IOC * AR A_BLOCK_ACK * !(AR C_IOC)</td><td></td><td>X</td></tr>
<tr><td>751A (AR C)</td><td>AR C_IOC</td><td></td><td></td><td>X</td><td>N/A</td></tr>
</table>

Trip Equations

In addition to using each relay's timed phase and ground overcurrent element (51P and 51G) and undervoltage elements (27YA, 27YB, 27YC, 27YAB, 27YBC and 27YCA), the GOOSE messages exchanged are incorporated into the trip equations of each relay. The first set of parentheses in the trip

equations includes the trip operation using the TOC and loss of potential settings as outlined in Table 2 and Table 4. The second set of parentheses pertain to the GOOSE protection scheme.

Trip equation of SEL-351A (AR A)
(51P + 51G + 27YA + 27YB + 27YC + 27YAB + 27YBC + 27YCA) * (!AR B_IOC)

The second set of parentheses is used to block the trip of AR A if the IOC element of AR B picks up, which would mean the fault is downstream of AR B. In this manner, AR A can remain closed for the fault without shifting to a slower TOC curve.

Trip equation of SEL-651R (AR B)
(51P + 51G + 27YA + 27YB + 27YC + 27YAB + 27YBC + 27YCA) + (AR B_IOC * AR A_BLOCK_ACK * !AR C_IOC)

Alternatively, the second set of parentheses allows AR B to trip if its own IOC element picks up, AR A has been blocked and the IOC element of AR C has not picked up, which confirms that the fault location is between AR B and AR C.

Trip equation of SEL-751A (AR C)
(51P + 51G + 27YA + 27YB + 27YC + 27YAB + 27YBC + 27YCA) + (AR B_IOC * AR A_BLOCK_ACK * !AR C_IOC)

The second set of parentheses allows AR C to trip since the logic signal confirms that the fault location is between AR B and AR C.

IEC61850-Based Protection Coordination Results

For the purpose of testing the IEC61850-based protection co-ordination scheme, two sets of LLLG faults, LL faults and LG faults were applied, with zero fault impedance and a 2 ohm fault impedance. All faults were for a duration of 500 cycles. Table 7 shows that AR B and AR C tripped for a bolted LLLG fault at location 1 and AR A remains closed. Note that due to the faster fault detection and clearing, the BESS can now ride-through a bolted LLLG fault, as shown in Figure 6.

Table 7. Trip Times and Communication Delays for Bolted LLLG Fault (Scheme 2)

AR A Trip Time (s)	*AR B Trip Time (s)*	*AR C Trip Time (s)*	*BESS Trip Time (s)*	*Time Lapse of GOOSE Block Signal from AR B to AR A (ms)*
N/A	0.0657	0.0956	N/A	9

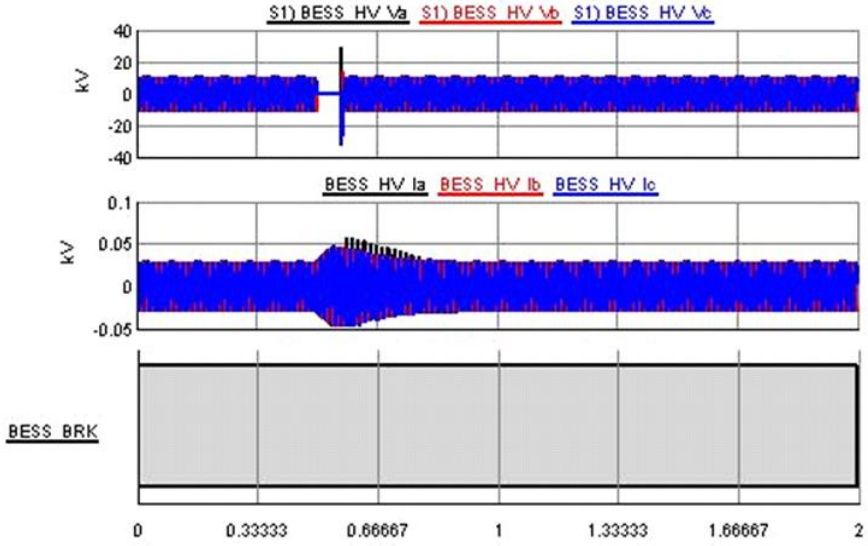

Figure 6. BESS - Bolted LLLG - Voltage, current and breaker status at HV terminal (Scheme 2)

COMPARISION RESULTS

Table 8 and Table 9 show the trip times for all fault cases that were performed. The results obtained from the testing of Scheme 1 shows that the average time taken for an AR to coordinate with an upstream AR through simulated CSC scheme was on average 44 ms. On the other hand, upstream relay coordination with GOOSE messaging could be achieved on average in 8 ms. Due to faster coordination with the upstream relay, trip time of the upstream relay closest to the fault (AR B) improves from an average of 357 ms to 70 ms and the trip time of the downstream relay (AR C) improves from an average of 30 s to 100 ms. It is also shown that a faster fault detection and clearing led to a successful BESS ride-through in all cases.

Table 8. Simulated CSC-Based Trip Times for All Test Cases (Scheme 1)

Test Case	*Fault Type*	*Fault Impedance (ohms)*	*Time for TOC Shift - AR B to AR A (ms)*	*AR A Trip Time (s)*	*AR B Trip Time (s)*	*AR C Trip Time (s)*	*BESS Trip Time (s)*
SIM_1.1	LLLG	1.00E-08	38.6	N/A	0.2917	30.06	0.2321
SIM_1.2	LL (AB)	1.00E-08	39.6	N/A	0.2253	30.3	N/A
SIM_1.3	LG (AG)	1.00E-08	44.8	N/A	0.3167	30.39	N/A
SIM_1.4	LLLG	2	45.1	N/A	0.417	30.48	N/A
SIM_1.5	LL (AB)	2	44	N/A	0.3172	30.39	N/A
SIM_1.6	LG (AG)	2	49.9	N/A	0.5752	30.65	N/A

Table 9. IEC61850-Based Trip Times for All Test Cases (Scheme 2)

Test Case	*Fault Type*	*Fault Impedance (ohms)*	*Time for GOOSE Block Signal - AR B to AR A (ms)*	*AR A Trip Time (s)*	*AR B Trip Time (s)*	*AR C Trip Time (s)*	*BESS Trip Time (s)*
HIL_1.1	LLLG	1.00E-08	9	N/A	0.0657	0.0956	N/A
HIL_1.2	LL (AB)	1.00E-08	6	N/A	0.0676	0.0981	N/A
HIL_1.3	LG (AG)	1.00E-08	8	N/A	0.0697	0.1014	N/A
HIL_1.4	LLLG	2	8	N/A	0.0824	0.099	N/A
HIL_1.5	LL (AB)	2	7	N/A	0.0794	0.1035	N/A
HIL_1.6	LG (AG)	2	8	N/A	0.0563	0.1041	N/A

CONCLUSIONS

Using IEC61850-based communications for fault detection and restoration can provide value in enhancing trip time of the relay closest to the fault and the immediate downstream relay. Faster fault detection and clearing time leads to conditions where DERs can now effectively ride-through fault scenarios (for downstream or adjacent feeder faults). It was also shown that, although enhancing communication system latency can improve CSC scheme, using IEC61850-based communications offers more comprehensive and versatile protection coordination schemes, agnostic to relay vendors, power system topologies, and outside of proprietary methods.

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